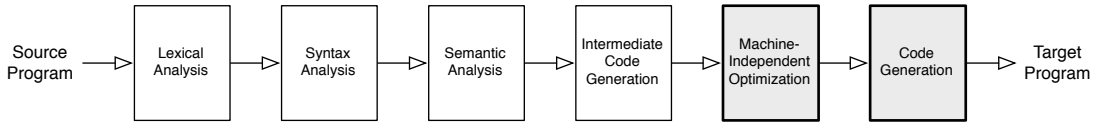
HW 11: More Dataflow Fun and Tiling

CSCI 434T
Fall, 2011

Overview



Not much new this week, although I want to at least briefly examine other code generation schemes beyond translating to TAC and then x86.

Readings

- From last week: Dragon 9.3 – 9.5.2
- Dragon 8.9 – 8.9.2

Exercises

1. Be prepared to tell me the following about PA 4:
   - How will you represent the dataflow facts for each required analysis in your compiler?
   - How will you use them to perform each required optimization on a TAC list?
2. Number 5 from last week.
3. Number 6 from last week.
4. Dragon 8.9.1.
   - For (a) and (c), assume all variables are stored at global memory locations. For (b), assume `x`, `y`, and `z` are at global memoery locations, and `i`, `j`, and `k` are locals stored relative to the stack pointer, as in the example from the book.
   - You may wish to add an additional tile form to dereference an address stored in a register.

   Reflect on the relative merits of Tiling vs. TAC. What do you see as the strengths/weaknesses of each?