1.) Suppose you are creating a cache with a data capacity of 32KBytes where each cache block is 64 Bytes. Assuming a 32-bit address, find the total number of bits needed to store both data and meta-data if the cache is organized as a direct-mapped cache. Perform the same calculations for a 2-way set associative cache. Show your work.

2.) How many bits are used for tag, index, and block fields given a 32 bit address and a 4096KByte 8-way set associative cache with 256Byte lines? Show your work.

3.) You are given a 64 byte cache with a 4 byte cache block size. It is direct mapped.
a) Label the following references as hits or misses.

Addr (in decimal)	Addr (in hexadecimal)	Hit or Miss
13	D	
116	74	
161	A1	
112	70	
15	F	
258	102	
129	81	
257	101	
75	4B	
256	100	
64	40	
14	E	

b) Show the final state of the cache. (You should specify the range of byte addresses in each row of the cache.)

c) What is the miss rate for this stream of references?

4) You are given a 64 byte cache with a 4 byte cache block size. It is **4-way set associative**. Assume LRU replacement.
a) Label the following references as hits or misses.

Addr (in decimal)	Addr (in hexadecimal)	Hit or Miss
13	D	
116	74	
161	A1	
112	70	
15	F	
258	102	
129	81	
257	101	
75	4B	
256	100	
64	40	
14	E	

b) Show the final state of the cache. (You should specify the range of byte addresses in each row of the cache.)

c) What is the miss rate for this stream of references?

5.) You are given a 16 byte cache with a 4 byte cache block size. It is **fully associative**. Assume LRU replacement.

a) Label the following references as hits or misses.

Addr (in decimal)	Addr (in hexadecimal)	Hit or Miss
13	D	
116	74	
161	A1	
112	70	
15	F	
258	102	
129	81	
257	101	
75	4B	
256	100	
64	40	
14	E	

b) Show the final state of the cache. (You should specify the range of byte addresses in each row of the cache.)

c) What is the miss rate for this stream of references?