Virtual Memory

CSCI 237: Computer Organization 30th Lecture, Monday, November 17, 2025

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lides originally designed by Bryant and O'Hallaron @ CMU for use with Computer Systems: A Programmer's Perspective, Third Editio

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Last Time: Caches

- Cache memory organization and operation (Ch 6.4)
- Caches in real systems
- Performance impact of caches
 - The memory mountain

Administrative Details

- Read CSAPP 9.1-9.6 (Ch. 9 sections are short)
- Lab #5 due Tueday at 11pm
- Sign up for partner on lab #6 by Wednesday at 8am
- Colloquium talk on Tuesday at 2:35pm in Wege
 - David Paulius, postdoc in Intelligent Robot Lab at Brown University
 - "Object-level Planning: Bridging Human Knowledge and Task and Motion Planning"
- Book extra credit
 - Need to sign up at least week in advance
 - Last days to talk to me are reading period

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Today: Virtual Memory

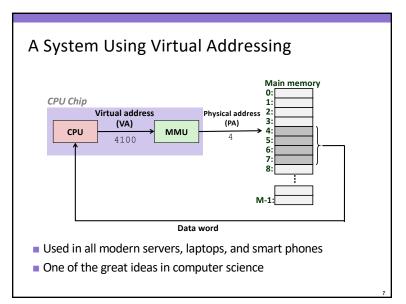
- Address spaces (Ch 9.2)
- VM as a tool for caching (Ch 9.3)
- VM as a tool for memory management (Ch 9.4)
- VM as a tool for memory protection (Ch 9.5)
- Address translation (Ch 9.6)

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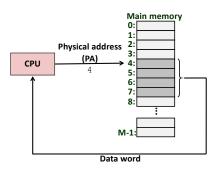
Question: How Does This Work?! Process 1 Process 2 Process n 00007FFFFFFFFFF 00007FFFFFFFFFF Stack Stack Shared Libraries Shared Shared Libraries Libraries Data Data Data Text 400000 000000 400000 **Solution: Virtual Memory**

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A System Using Physical Addressing



Used in "simple" systems like embedded microcontrollers in devices like cars, elevators, and digital picture frames

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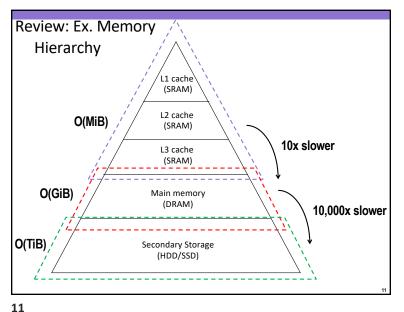
Address Spaces: Terminology

- Linear address space: Ordered set of contiguous nonnegative integer addresses (we always assume this): {0, 1, 2, 3 ...}
- Virtual address space: Set of N = 2ⁿ virtual addresses {0, 1, 2, 3, ..., N-1}
- Physical address space: Set of M = 2^m physical addresses

{0, 1, 2, 3, ..., M-1}

Why Virtual Memory (VM)?

- Uses main memory efficiently
 - Use DRAM as a cache for parts of a virtual address space
- Simplifies memory management
 - Each process gets the same uniform linear address space
- Isolates address spaces
 - Enables multiple processes to execute simultaneously
 - One process can't interfere with another's memory
 - Processes can allocate memory dynamically
 - User program cannot access privileged kernel information and
- Total virtual memory in use can exceed physical memory



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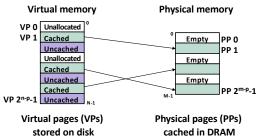
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VM as a Tool for Caching

- Conceptually, *virtual memory* is an array of N contiguous bytes stored on disk.
- The contents of the array on disk are cached in physical memory (DRAM cache)
 - These cache blocks are called pages (size is P = 2^p bytes)



DRAM Cache Organization

- DRAM cache organization driven by the enormous miss penalty
 - DRAM is about 10x slower than SRAM
 - Disk is about 10,000x slower than DRAM
- Consequences
 - Large page (block) size: typically 4 KB, sometimes 4 MB
 - Fully associative
 - Any VP can be placed in any PP
 - Requires a "large" mapping function different from cache memories
 - Highly sophisticated, expensive replacement algorithms
 - Too complicated and open-ended to be implemented in hardware
 - Write-back rather than write-through

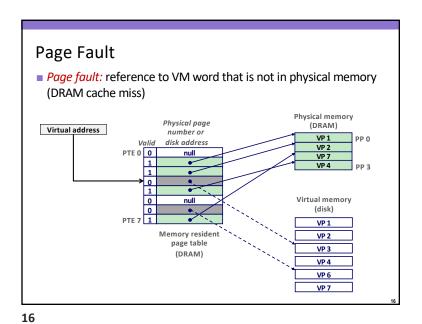
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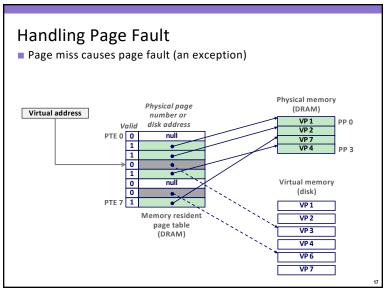
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Page Hit Page hit: reference to VM word that is in physical memory (DRAM cache hit) Physical memory Physical page Virtual address (DRAM) number or VP 1 PP 0 Valid disk address VP 2 PTE 0 0 null VP 7 VP 4 0 1 Virtual memory 0 (disk) VP 1 Memory resident VP 2 page table VP3 (DRAM) VP 4 VP 6 VP 7

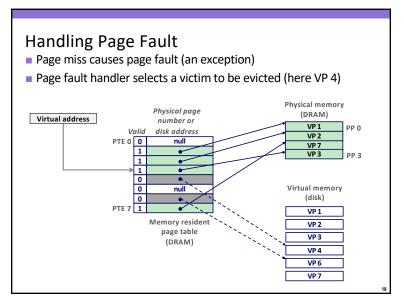
Enabling Data Structure: Page Table ■ A page table is an array of page table entries (PTEs) that maps virtual pages to physical pages. Per-process kernel (i.e., OS) data structure in DRAM Physical memory Physical page (DRAM) number or VP 1 Valid disk address VP 2 PTE 0 0 VP 7 Virtual memory null (disk) VP 1 Memory resident VP 2 page table VP 3 (DRAM) VP 4 VP 6

VP 7



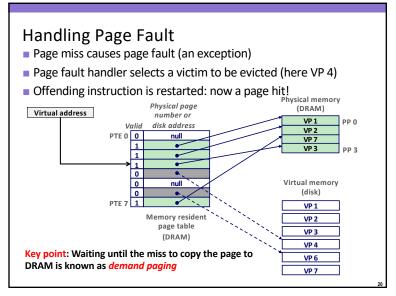


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Handling Page Fault ■ Page miss causes page fault (an exception) ■ Page fault handler selects a victim to be evicted (here VP 4) Physical memory Physical page (DRAM) Virtual address number or VP 1 disk address Valid VP 2 null VP 7 VP 4 Virtual memory null (disk) VP 1 Memory resident VP 2 page table VP 3 (DRAM) VP 4 VP 6 VP 7

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Allocating Pages Allocating a new page (VP 5) of virtual memory. Physical memory Physical page (DRAM) number or VP1 disk address VP 7 VP3 0 Virtual memory (disk) VP 1 Memory resident VP 2 page table VP3 (DRAM) VP 4 VP 6 VP 7

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Locality to the Rescue Again!

Virtual memory seems terribly inefficient, but it works because of locality.

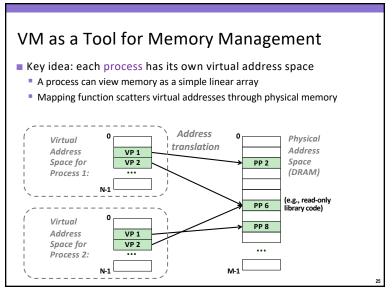
- At any point in time, programs tend to access a set of active virtual pages called the working set
 - Programs with better temporal locality will have smaller working sets
- If (working set size < main memory size)
 - Good performance for one process after initial compulsory misses
- If (SUM(working set sizes) > main memory size)
 - Thrashing: Performance meltdown where pages are swapped (copied) in and out continuously

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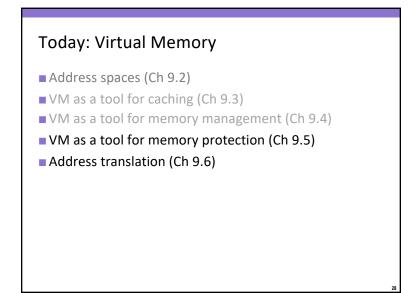
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VM as a Tool for Memory Management Simplifies memory allocation Each virtual page can be mapped to any physical page A virtual page can be stored in different physical pages at different times Allows sharing code and data among processes Why? Can map virtual pages to the same physical page (here: PP 6) Address Physical Virtual translation Address Address VP 1 Space Space for VP 2 (DRAM) Process 1: (e.g., read-only library code) Virtual VP 1 Address VP 2 Space for Process 2:

VM as a Tool for Memory Protection ■ General Idea: Extend PTEs with permission bits MMU checks these bits on each access Physical READ WRITE EXEC Address Address Space Process i: VP 0: Yes VP 1: Yes PP 4 Yes PP 2 No PP 2 PP 4 PP 6 SUP READ WRITE EXEC Address Process i: PP 8 VP 0: PP 9 No Yes No PP 9 VP 1: Yes PP 6 Yes Yes Yes PP 11 PP 11 Yes Yes

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Summary of Address Translation Jargon

- Basic Parameters
 - N = 2ⁿ: Number of addresses in virtual address space
 - M = 2^m: Number of addresses in physical address space
 - P = 2^p: Page size (in bytes) of physical and virtual pages
- Components of the virtual address (VA)
 - **VPN**: Virtual page number
 - **VPO**: Virtual page offset
 - TLBI: TLB (Translation Lookaside Buffer) index
 - TLBT: TLB tag
- Components of the physical address (PA)
 - **PPN:** Physical page number
 - **PPO**: Physical page offset (same as VPO)

VM Address Translation (formally)

- Virtual Address Space
- $V = \{0, 1, ..., N-1\}$
- Physical Address Space
 - $P = \{0, 1, ..., M-1\}$
- Address Translation. $MAP: V \rightarrow P \cup \{\emptyset\}$
 - For virtual address a:

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- MAP(a) = a' if data at virtual address a in V is at physical address a' in P
- MAP(a) = Ø if data at virtual address a is not in physical memory (either unallocated or stored on disk)